Search History

STN
(HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC)
7/22/06

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     (FILE 'HOME' ENTERED AT 09:31:44 ON 21 JUL 2006)

     FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2, INPADOC' ENTERED AT
     09:32:14 ON 21 JUL 2006
L1        528080 S (WAFER#)
L2         78348 S (SI OR SILICON)(8A)(SINGLE(W)CRYSTAL# OR MONO(W)CRYSTAL#)
L3         16806 S (DOP?)(8A)(NITROGEN)
L4         44134 S (CZ OR CZOCHRALSKI)
L5      12584170 S (CONTROL? OR ALTER? OR VARY? OR MANIPULAT?)
L6         30781 S (DEFEAT? OR ELIMINAT? OR LOWER? OR REDUC? OR DECREAS?)(8A)(VO

=> s l1 and l2 and l3 and l4 and l5 and l6
L7            43 L1 AND L2 AND L3 AND L4 AND L5 AND L6

=> s (slic? or cut?)
L8       2496368 (SLIC? OR CUT?)

=> s l7 and l8
L9            38 L7 AND L8

=> d l9 1-38 abs,bib

L9   ANSWER 1 OF 38  USPATFULL on STN
AB     There is provided a method for manufacturing a silicon wafer
       or a silicon epitaxial wafer capable of imparting an excellent
       IG capability thereto in a stable manner by simultaneously realizing
       higher density of oxide precipitates and larger sizes thereof at a stage
       prior to a device fabrication process. The present invention is a method
       for manufacturing a silicon wafer wherein the silicon
       wafer is subjected to heat treatment to impart a gettering
       capability thereto comprising at least the following three steps of: a
       temperature raising step A for generating oxygen precipitation nuclei; a
       temperature raising step B for growing the oxygen precipitation nuclei;
       and a constant temperature keeping step C for growing the oxygen
       precipitation nuclei into oxide precipitates of larger sizes.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN     2006:155220  USPATFULL
TI     Methods for manufacturing silicon wafer and silicon epitaxial
       wafer, and silicon epitaxial wafer
IN     Takeno, Hiroshi, Annaka-shi, JAPAN
PI     US 2006130736      A1   20060622
AI     US 2006-339672     A1   20060126 (11)
RLI    Division of Ser. No. US 2004-482843, filed on 6 Jan 2004, GRANTED, Pat.
       No. US 7033962
PRAI   JP 2001-209160      20010710
       JP 2001-296743      20010927
       JP 2001-296744      20010927
       JP 2001-296745      20010927
DT     Utility
FS     APPLICATION
LREP   RADER FISHMAN & GRAUER PLLC, LION BUILDING, 1233 20TH STREET N.W., SUITE
       501, WASHINGTON, DC, 20036, US
CLMN   Number of Claims: 15
ECL    Exemplary Claim: 1-8
DRWN   14 Drawing Page(s)
LN.CNT 2424
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9   ANSWER 2 OF 38  USPATFULL on STN
AB     The present invention provides an annealed wafer which has a
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wafer surface layer serving as a device fabricating region and having an excellent oxide film dielectric breakdown characteristic, and a wafer bulk layer in which oxide precipitates are present at a high density at the stage before the wafer is loaded into the device fabrication processes to give an excellent IG capability, and a method for manufacturing the annealed wafer. The present invention is directed to an annealed wafer obtained by performing heat treatment on a silicon wafer manufactured from a silicon single crystal grown by the Czochralski method, wherein a good chip yield of an oxide film dielectric breakdown characteristic in a region having at least a depth of up to 5 μm from a wafer surface is 95% or more, and a density of oxide precipitates detectable in the wafer bulk and each having a size not smaller than a size showing a gettering capability is not less than 1+10.sup.9/cm.sup.3.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2006:89836 USPATFULL
TI Annealed wafer and anneald wafer manufacturing method
IN Takeno, Hiroshi, Gunma, JAPAN
Sakurada, Masahiro, Fukushima, JAPAN
Kobayashi, Takeshi, Fukushima, JAPAN
PI US 2006075957 A1 20060413
AI US 2003-530557 A1 20030929 (10)
WO 2003-JP12396 20030929
20050407 PCT 371 date
PRAI JP 2002-294713 20021008
DT Utility
FS APPLICATION
LREP RADER FISHMAN & GRAUER PLLC, LION BUILDING, 1233 20TH STREET N.W., SUITE 501, WASHINGTON, DC, 20036, US
CLMN Number of Claims: 25
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 1453
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 3 OF 38 USPATFULL on STN

AB There are disclosed a silicon wafer for epitaxial growth wherein the wafer is produced by slicing a silicon single crystal grown with doping nitrogen according to the Czochralski method (CZ method) in the region where at least the center of the wafer becomes V region in which the void type defects are generated, and wherein the number of defects having an opening size of 20 nm or less among the void type defects appearing on the surface of the wafer is 0.02/cm.sup.2 or less, and an epitaxial wafer wherein an epitaxial layer is formed on the silicon wafer for epitaxial growth. Thereby, there can be produced an epitaxial wafer having a high gettering capability wherein very few SF exist in the epitaxial layer easily at high productivity and at low cost.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2005:243977 USPATFULL
TI Silicon wafer for epitaxial growth, epitaxial wafer, and its manufacturing method
IN Hoshi, Ryoji, Fukushima, JAPAN
Sonokawa, Susumu, Fukushima, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 2005211158 A1 20050929
AI US 2003-520099 A1 20030708 (10)

WO 2003-JP8671 20030708
20050104 PCT 371 date
PRAI JP 2002-204703 20020712
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320, US
CLMN Number of Claims: 30
ECL Exemplary Claim: 1-11
DRWN 6 Drawing Page(s)
LN.CNT 849
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 4 OF 38 USPATFULL on STN
AB A process for producing a single crystal silicon wafer comprising a front surface, a back surface, a lateral surface joining the front and back surfaces, a central axis perpendicular to the front and back surfaces, and a segment which is axially symmetric about the central axis extending substantially from the front surface to the back surface in which crystal lattice vacancies are the predominant intrinsic point defect, the segment having a radial width of at least about 25% of the radius and containing agglomerated vacancy defects and a residual concentration of crystal lattice vacancies wherein (i) the agglomerated vacancy defects have a radius of less than about 70 nm and (ii) the residual concentration of crystal lattice vacancy intrinsic point defects is less than the threshold concentration at which uncontrolled oxygen precipitation occurs upon subjecting the wafer to an oxygen precipitation heat treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:186064 USPATFULL
TI Process for preparing single crystal silicon having improved gate oxide integrity
IN Falster, Robert J., London, UNITED KINGDOM
Voronkov, Vladimir V., Merano, ITALY
Mutti, Paolo, Milan, ITALY
Bonoli, Francesco, Novara, ITALY
PA MEMC Electronic Materials, Inc., St. Peters, MO, UNITED STATES, 63376 (non-U.S. corporation)
PI US 2005160967 A1 20050728
AI US 2005-89102 A1 20050324 (11)
RLI Division of Ser. No. US 2002-39196, filed on 2 Jan 2002, PENDING
PRAI US 2001-259362P 20010102 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102, US
CLMN Number of Claims: 26
ECL Exemplary Claim: 1
DRWN 17 Drawing Page(s)
LN.CNT 1886
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 5 OF 38 USPATFULL on STN
AB A silicon single crystal wafer grown by the CZ method, which is doped with nitrogen and has an N-region for the entire plane and an interstitial oxygen concentration of 8 ppma or less, or which is doped with nitrogen and has an interstitial oxygen concentration of 8 ppma or less, and in which at least void type defects and dislocation clusters are eliminated from the entire plane, and a method for producing the same. Thus, there are provided a defect-free silicon single crystal wafer having an N-region for the entire plane,

in which void type defects and dislocation clusters are eliminated, produced by the CZ method under readily controllable stable production conditions with a wide controllable range, and a method producing the same.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:13194 USPATFULL
TI Silicon single crystal wafer and production method thereof and soi wafer
IN Iida, Makoto, Gunma, JAPAN
Kimura, Masanori, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6843847 B1 20050118
WO 2001036719 20010525
AI US 2001-869912 20010709 (9)
WO 2000-JP7809 20001107
20010709 PCT 371 date
PRAI JP 1999-322487 19991112
DT Utility
FS GRANTED
EXNAM Primary Examiner: Kunemund, Robert
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 21
ECL Exemplary Claim: 1
DRWN 2 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 884
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 6 OF 38 USPATFULL on STN
AB A method for producing a silicon ingot through pulling up a silicon single crystal according to the Czochralski method, wherein the silicon single crystal is pulled up while being doped with nitrogen in such a condition as to form a part having a nitrogen content of 5+10.sup.13 atoms/cm.sup.3 to 1+10.sup.15 atoms/cm.sup.3. A silicon wafer having a nitrogen content of 5+10.sup.13 atoms/cm.sup.3 to 1+10.sup.15 atoms/cm.sup.3 which is suitable for being treated with heat in a non-oxidizing atmosphere is manufactured of an ingot produced by using the method. The method can be used for producing a silicon wafer being doped with nitrogen and having satisfactory characteristics for use in a semiconductor device.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:250070 USPATFULL
TI Silicon wafer and method for manufacture thereof, and method for evaluation of silicon wafer
IN Komiya, Satoshi, Kanagawa, JAPAN
Yoshino, Shiro, Hiratsuka, JAPAN
Danbata, Masayoshi, Kanagawa, JAPAN
Hayashida, Kouichirou, Kanagawa, JAPAN
PA Komatsu Denshi Sinzoku Kabushiki, Kanagawa, JAPAN (non-U.S. corporation)
PI US 6800132 B1 20041005
WO 2001016409 20010308
AI US 2002-49875 20020212 (10)
WO 2000-JP5738 20000825
PRAI JP 1999-241186 19990827
DT Utility
FS GRANTED
EXNAM Primary Examiner: Kunemund, Robert
LREP Welsh & Katz, Ltd.
CLMN Number of Claims: 14
ECL Exemplary Claim: 1
DRWN 16 Drawing Figure(s); 14 Drawing Page(s)

LN.CNT 664
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 7 OF 38 USPATFULL on STN
AB There is provided a method for manufacturing a silicon wafer or a silicon epitaxial wafer capable of imparting an excellent IG capability thereto in a stable manner by simultaneously realizing higher density of oxide precipitates and larger sizes thereof at a stage prior to a device fabrication process. The present invention is a method for manufacturing a silicon wafer wherein the silicon wafer is subjected to heat treatment to impart a gettering capability thereto comprising at least the following three steps of: a temperature raising step A for generating oxygen precipitation nuclei; a temperature raising step B for growing the oxygen precipitation nuclei; and a constant temperature keeping step C for growing the oxygen precipitation nuclei into oxide precipitates of larger sizes.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:221464 USPATFULL
TI Silicon wafer manufacturing method, silicon epitaxial wafer manufacturing method, and silicon epitaxial wafer
IN Takeno, Hiroshi, Gunma, JAPAN
PI US 2004171234 A1 20040902
US 7033962 B2 20060425
AI US 2004-482843 A1 20040106 (10)
WO 2002-JP5000 20020530
PRAI JP 2001-209160 20010710
JP 2001-296743 20010927
JP 2001-296744 20010927
JP 2001-296745 20010927
DT Utility
FS APPLICATION
LREP Rader Fishman & Grauer, Suite 501, 1233 20th Street NW, Washington, DC, 20036
CLMN Number of Claims: 34
ECL Exemplary Claim: 1
DRWN 14 Drawing Page(s)
LN.CNT 2580
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 8 OF 38 USPATFULL on STN
AB The present invention relates to single crystal silicon, ingot or wafer form, which contains an axially symmetric region in which vacancies are the predominant intrinsic point defect, is substantially free of oxidation induced stacking faults and is nitrogen doped to stabilize oxygen precipitation nuclei therein, and a process for the preparation thereof.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:12593 USPATFULL
TI Nitrogen-doped silicon substantially free of oxidation induced stacking faults
IN Haga, Hiroyo, Tochigi Prefecture, JAPAN
Aoshima, Takaaki, Tochigi Prefecture, JAPAN
Banan, Mohsen, St. Peters, MI, UNITED STATES
PI US 2004009111 A1 20040115
AI US 2003-380806 A1 20030730 (10)
WO 2001-US27049 20010830
PRAI JP 2000-283033 20000919
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102

CLMN Number of Claims: 56
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 1133
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 9 OF 38 USPATFULL on STN
AB There are provided a silicon wafer for epitaxial growth wherein a void type defect is not exposed on the surface where an epitaxial layer is grown, and a method for producing an epitaxial wafer comprising measuring the number of the void type defects exposed on the surface of a silicon wafer and/or the number of the void type defects which exist in the part to the depth of at least 10 nm from the surface of the silicon wafer, choosing the silicon wafer wherein the number of these void type defects is smaller than the predetermined value, and growing an epitaxial layer on the surface of the chosen silicon wafer. Thereby, there can be provided a silicon wafer for epitaxial growth wherein generation of SF is reduced and epitaxial wafer, and a method for producing it.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:260456 USPATFULL
TI Silicon wafer for epitaxial wafer, epitaxial wafer, and method of manufacture thereof
IN Kimura, Akihiro, Gunma, JAPAN
Sato, Hideki, Gunma, JAPAN
Kono, Ryuji, Gunma, JAPAN
Kato, Masahiro, Gunma, JAPAN
Tamatsuka, Masaro, Gunma, JAPAN
PA Shin Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6626994 B1 20030930
WO 2001038611 20010531
AI US 2001-890007 20010724 (9)
WO 2000-JP8204 20001121
PRAI JP 1999-334040 19991125
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Hogan & Hartson, LLP
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 19 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 623
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 10 OF 38 USPATFULL on STN
AB The present invention provides a silicon single crystal wafer having a diameter of 300 mm or more and having a defect-free layer containing no COP for a depth of 3 μm or more from a surface and a method for producing a silicon single crystal, wherein, when a silicon single crystal having a diameter of 300 mm or more is pulled with nitrogen doping by the CZ method, the crystal is grown with a value of V/G [mm.sup.2/K.cndot.min] of 0.17 or less, where V [mm/min] is a pulling rate, and G [K/mm] is an average of temperature gradient in the crystal along a pulling axis from the melting point of silicon to 1400° C. Thus, there are established conditions for pulling a silicon single crystal and conditions for heat treatment of wafer for obtaining a silicon single crystal wafer having a defect-free layer free from COP for a sufficient depth of the surface layer by pulling a silicon single crystal having a diameter of 300 mm or more, processing the

crystal into wafers and subjecting the wafers to the heat treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:248088 USPATFULL
TI Silicon single crystal wafer having void denuded zone on the surface and diameter of above 300mm and its production method
IN Iida, Makoto, Gunma, JAPAN
PI US 2003172865 A1 20030918
US 6902618 B2 20050607
AI US 2003-344423 A1 20030212 (10)
WO 2002-JP5692 20020607
PRAI JP 2001-181587 20010615
DT Utility
FS APPLICATION
LREP HOGAN & HARTSON L.L.P., 500 S. GRAND AVENUE, SUITE 1900, LOS ANGELES, CA, 90071-2611
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN No Drawings
LN.CNT 433
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 11 OF 38 USPATFULL on STN
AB According to the present invention, there are provided a method for producing a silicon single crystal wafer which contains oxygen induced defects by subjecting a silicon single crystal wafer containing interstitial oxygen to a heat treatment wherein the heat treatment includes at least a step of performing a heat treatment using a resistance-heating type heat treatment furnace and a step of performing a heat treatment using a rapid heating and rapid cooling apparatus, and a silicon single crystal wafer produced by the method. There can be provided a method for producing a silicon single crystal wafer which has a DZ layer of higher quality compared with a conventional wafer in a wafer surface layer part and has oxygen induced defects at a sufficient density in a bulk part and the silicon single crystal wafer .

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:235983 USPATFULL
TI Method for manufacturing single-crystal-silicon wafers
IN Kobayashi, Norihiro, Gunma, JAPAN
Tamatsuka, Masaro, Gunma, JAPAN
Nagoya, Takatoshi, Gunma, JAPAN
PI US 2003164139 A1 20030904
US 6805743 B2 20041019
AI US 2003-333970 A1 20030124 (10)
WO 2001-JP6274 20010719
PRAI JP 2000-229522 20000728
DT Utility
FS APPLICATION
LREP HOGAN & HARTSON L.L.P., 500 S. GRAND AVENUE, SUITE 1900, LOS ANGELES, CA, 90071-2611
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 552
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 12 OF 38 USPATFULL on STN
AB The present invention provides a CZ silicon wafer, wherein the wafer includes rod-like void defects and/or plate-like void defects inside thereof, and a CZ silicon wafer, wherein the silicon wafer includes void defects inside the wafer, a maximum value of a ratio between long side length L1 and short side length L2 (L1/L2) in an optional rectangle circumscribed the void defect image projected on an optional {110} plane is 2.5 or more, and the silicon wafer including rod-like void defects and/or plate-like void defects inside the wafer, wherein a void defect density of the silicon wafer at a depth of from the wafer surface to at least 0.5 μm after the heat treatment is 1/2 or less than that of inside the wafer. According to this, the silicon wafer, which is suitable for expanding reducing effect of void defects by heat treatment up to a deeper region, can be obtained.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:203182 USPATFULL
TI Silicon wafer
IN Kato, Masahiro, Annaka, JAPAN
Tamatsuka, Masaro, Annaka, JAPAN
Imai, Osamu, Annaka, JAPAN
Kimura, Akihiro, Annaka, JAPAN
Yoshida, Tomosuke, Annaka, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6599603 B1 20030729
WO 2000052236 20000908
AI US 2000-673955 20001024 (9)
WO 2000-JP1125 20000225
PRAI JP 1999-57738 19990304
DT Utility
FS GRANTED
EXNAM Primary Examiner: Lam, Cathy; Assistant Examiner: Stein, Stephen
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 12
ECL Exemplary Claim: 2
DRWN 6 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 489
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 13 OF 38 USPATFULL on STN
AB A silicon semiconductor substrate which realises a defect-free region of void type crystals to a greater depth and allows the duration of production to be decreased and a method for the production thereof are provided.

Means to fulfil the task: A silicon semiconductor substrate derived from a silicon single crystal grown by the Czochralski method or the magnetic field-applied Czochralski method, which is obtainable by using a silicon semiconductor substrate satisfying the relational expression, $0.2 \geq V/S/R$, providing V denotes the volume of void type defects, S the surface area thereof, and R the radius of spherical defects presumed to have the same volume as the void type defects having the volume of V, and heat-treating this substrate at a temperature exceeding 1150° C.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:194709 USPATFULL
TI Silicon semiconductor substrate and method for production thereof
IN Tachikawa, Akiyoshi, Yamaguchi, JAPAN
Ishisaka, Kazunori, Yamaguchi, JAPAN
PA WACKER SILTRONIC GESELLSCHAFT FUR HALBLEITERMATERIALIEN AG (non-U.S.

corporation)
PI US 2003134520 A1 20030717
US 6767848 B2 20040727
AI US 2002-241180 A1 20020911 (10)
PRAI JP 2001-280460 20010914
DT Utility
FS APPLICATION
LREP WILLIAM COLLARD, COLLARD & ROE, P.C., 1077 NORTHERN BOULEVARD, ROSLYN, NY, 11576
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN No Drawings
LN.CNT 1079
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 14 OF 38 USPATFULL on STN
AB According to the present invention, there is disclosed a silicon single crystal wafer grown according to the CZ method which is a wafer having a diameter of 200 mm or more produced from a single crystal grown at a growth rate of 0.5 mm/min or more without doping except for a dopant for controlling resistance, wherein neither an octahedral void defect due to vacancies nor a dislocation cluster due to interstitial silicons exists as a grown-in defect, and a method for producing it. There can be provided a high quality silicon single crystal wafer having a large diameter wherein a silicon single crystal in which both of octahedral void defects and dislocation clusters which are growth defects are substantially eliminated is grown at higher rate compared with the conventional method by the usual CZ method, and furthermore by controlling a concentrations of interstitial oxygen in the crystal to be low, a precipitation amount is lowered and ununiformity of BMD in a plane of the wafer is improved, and provided a method for producing it.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:156882 USPATFULL
TI Silicon single crystal wafer and method for manufacturing the same
IN Fusegawa, Izumi, Nishishirakawa-gun Fukushima, JAPAN
Kitagawa, Koji, Nishishirakawa-gun Fukushima, JAPAN
Hoshi, Ryoji, Nishishirakawa-gun Fukushima, JAPAN
Sakurada, Masahiro, Nishishirakawa-gun Fukushima, JAPAN
Ohta, Tomohiko, Nishishirakawa-gun Fukushima, JAPAN
PI US 2003106484 A1 20030612
US 6893499 B2 20050517
AI US 2002-312921 A1 20021226 (10)
WO 2001-JP5565 20010628
PRAI JP 2000-199226 20000630
DT Utility
FS APPLICATION
LREP HOGAN & HARTSON L.L.P., 500 S. GRAND AVENUE, SUITE 1900, LOS ANGELES, CA, 90071-2611
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 963
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 15 OF 38 USPATFULL on STN
AB An improved method of obtaining a wafer exhibiting high resistivity and high gettering effect while preventing the reduction of resistivity due to the generation of oxygen donors provided by: a) using the CZ method to grow a silicon single

crystal ingot having a resistivity of 100 Ω.multidot.cm or more, preferably 1000 Ω.multidot.cm, and an initial interstitial oxygen concentration of 10 to 40 ppma while doping the crystal with an electrically inactive material such as nitrogen, carbon, or tin, b) processing the ingot into a wafer, and c) subjecting the wafer to an oxygen precipitation heat treatment whereby the residual interstitial oxygen content in the wafer is reduced to about 8 ppma or less.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:156880 USPATFULL
TI High resistivity silicon wafer having electrically inactive dopant and method of producing same
IN Kononchuk, Oleg V., Brush Prairie, WA, UNITED STATES
Koveshnikov, Sergei V., Vancouver, WA, UNITED STATES
Radzimski, Zbigniew J., Brush Prairie, WA, UNITED STATES
Weaver, Neil A., Battle Ground, WA, UNITED STATES
PA SEH America, Inc. (U.S. corporation)
PI US 2003106482 A1 20030612
US 6673147 B2 20040106
AI US 2001-8404 A1 20011206 (10)
DT Utility
FS APPLICATION
LREP ALSTON & BIRD LLP, BANK OF AMERICA PLAZA, 101 SOUTH TRYON STREET, SUITE 4000, CHARLOTTE, NC, 28280-4000
CLMN Number of Claims: 33
ECL Exemplary Claim: 1
DRWN 1 Drawing Page(s)
LN.CNT 691
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 16 OF 38 USPATFULL on STN
AB A silicon semiconductor substrate is obtained by deriving a silicon semiconductor substrate from a silicon single crystal grown by the Czochralski method from a molten silicon containing not less than 1+10.sup.16 atoms/cm.sup.3 and not more than 1.5+10.sup.19 atoms/cm.sup.3 of nitrogen and heat-treating the silicon semiconductor substrate at a temperature of not less than 1000° C. and not more than 1300° C. for not less than one hour and is characterized by the fact that the density of crystal defects measuring not less than 0.1 μm as reduced to diameter is not more than 10.sup.4 pieces/cm.sup.3 at least in the region reaching a depth of 1 μm from the surface of the substrate and the nitrogen content at the center of thickness of the silicon semiconductor substrate is not less than 1+10.sup.13 atoms/cm.sup.3 and not more than 1+10.sup.16 atoms/cm.sup.3.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:102580 USPATFULL
TI Silicon semiconductor wafer and method for producing the same
IN Ikari, Atsushi, Chiba, JAPAN
Hasebe, Masami, Chiba, JAPAN
Nakai, Katsuhiko, Chiba, JAPAN
Sakamoto, Hikaru, Chiba, JAPAN
Ohashi, Wataru, Chiba, JAPAN
Hoshino, Taizo, Yamaguchi, JAPAN
Iwasaki, Toshio, Yamaguchi, JAPAN
PA Wacker NSCE Corporation, Tokyo, JAPAN (non-U.S. corporation)
PI US 6548886 B1 20030415
WO 9957344 19991111
AI US 2000-508467 20000310 (9)
WO 1999-JP2336 19990430
PRAI JP 1998-122284 19980501
JP 1998-224829 19980807

JP 1999-84915 19990326
JP 1999-84916 19990326
DT Utility
FS GRANTED
EXNAM Primary Examiner: Picardat, Kevin M.
LREP Wenderoth, Lind & Ponack, L.L.P.
CLMN Number of Claims: 26
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 3109
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 17 OF 38 USPATFULL on STN
AB A silicon single crystal wafer for epitaxial growth grown by the CZ method, which is doped with nitrogen and has a V-rich region over its entire plane, or doped with nitrogen, has an OSF region in its plane, and shows an LEP density of 20/cm.sup.2 or less or an OSF density of 1+10.sup.4/cm.sup.2 or less in the OSF region, epitaxial wafer utilizing the substrate, as well as methods for producing them and method for evaluating a substrate suitable for an epitaxial wafer. There are provided a substrate for an epitaxial wafer that suppresses crystal defects to be generated in an epitaxial layer when epitaxial growth is performed on a CZ silicon single crystal wafer doped with nitrogen and also has superior IG ability, epitaxial wafer utilizing the substrate, as well as methods for producing them and method for evaluating a substrate suitable for an epitaxial wafer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:102116 USPATFULL
TI Silicon single crystal wafer for epitaxial wafer, epitaxial wafer, and methods for producing the same and evaluating the same
IN Kimura, Akihiro, Gunma, JAPAN
Iida, Makoto, Gunma, JAPAN
Hayamizu, Yoshinori, Gunma, JAPAN
Aihara, Ken, Gunma, JAPAN
Kimura, Masanori, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6548035 B1 20030415
WO 2001027362 20010419
AI US 2001-868058 20010614 (9)
WO 2000-JP6965 20001005
PRAI JP 1999-294523 19991015
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 29
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 925
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 18 OF 38 USPATFULL on STN
AB A silicon wafer obtained by slicing a silicon single crystal ingot grown by the Czochralski method with or without nitrogen doping, wherein the silicon wafer has an NV-region, an NV-region containing an OSF ring region or an OSF ring region for its entire plane and has an interstitial oxygen concentration of 14 ppma or less, and a method for producing it, as well as a method for evaluating

defect regions of a silicon wafer. Thus, there are provided a silicon wafer that stably provides oxygen precipitation regardless of position in crystal or device production process, and a method for producing it. Further, defect regions of a silicon wafer of which pulling conditions are unknown and thus of which defect regions are also unknown can be evaluated.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:95797 USPATFULL
TI Silicon wafer and production method thereof and evaluation method for silicon wafer
IN Takeno, Hiroshi, Gunma, JAPAN
Shigeno, Hideki, Gunma, JAPAN
Iida, Makoto, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6544490 B1 20030408
WO 2001036718 20010525
AI US 2001-869932 20010709 (9)
WO 2000-JP7808 20001107
PRAI JP 1999-322242 19991112
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 9 Drawing Figure(s); 9 Drawing Page(s)
LN.CNT 906
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 19 OF 38 USPATFULL on STN
AB A silicon semiconductor substrate has a structure possessing oxygen precipitate defects fated to form gettering sites in a high density directly below the defect-free region of void type crystals. The silicon semiconductor substrate is formed by heat-treating a silicon semiconductor substrate derived from a silicon single crystal grown by the Czochralski method or the magnetic field-applied Czochralski method and characterized by satisfying the relational expression (Oi DZ)-(COP DZ)≤10 μm wherein Oi DZ denotes a defect-free zone of oxygen precipitate crystal defects and COP DZ denotes a region devoid of a void type defect measuring not less than 0.11 μm in size, and having not less than 5+10.sup.8 oxygen precipitate crystal defects per cm.sup.3. The method for making the substrate comprises the steps of deriving a silicon semiconductor substrate from a silicon single crystal grown by the Czochralski method or the magnetic field-applied Czochralski method using molten silicon containing not less than 5+10.sup.17 atoms and not more than 1.5+10.sup.19 atoms of nitrogen per cm.sup.3 and heat-treating the silicon semiconductor substrate in a non-oxidizing atmosphere at a highest final temperature of not lower than 1150° C. for not less than one hour.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:83135 USPATFULL
TI Silicon semiconductor substrate and preparation thereof
IN Tachikawa, Akiyoshi, Hikari, JAPAN
Ikari, Atsushi, Tokuyama, JAPAN
PA Wacker Siltronic Gesellschaft Fur Halbleitermaterialien AG (non-U.S. corporation)
PI US 2003056715 A1 20030327
AI US 2002-236273 A1 20020906 (10)
PRAI JP 2001-280459 20010914
DT Utility

FS APPLICATION
LREP Collard & Roe, 1077 Northern Blvd., Roslyn, NY, 11576
CLMN Number of Claims: 6
ECL Exemplary Claim: 1
DRWN No Drawings
LN.CNT 1007
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 20 OF 38 USPATFULL on STN
AB There is provided a method of producing a bonded SOI wafer wherein a silicon single crystal ingot is grown according to Czochralski method, the single crystal ingot is then sliced to produce a silicon single crystal wafer, the silicon single crystal wafer is subjected to heat treatment in a non-oxidizing atmosphere at a temperature of 1100° C. to 1300° C. for one minute or more and continuously to a heat treatment in an oxidizing atmosphere at a temperature of 700° C. to 1300° C. for one minute or more without cooling the wafer to a temperature less than 700° C. to provide a silicon single crystal wafer wherein a silicon oxide film is formed on the surface, and the resultant wafer is used as the bond wafer, and a bonded SOI wafer produced by the method. There can be provided a SOI wafer that has a SOI layer having few crystal defects, good surface roughness and high quality in high productivity, in high yield and with low cost.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:28176 USPATFULL
TI Method of producing a bonded wafer and the bonded wafer
IN Akiyama, Shoji, Gunma, JAPAN
Tamatsuka, Masaro, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd. (non-U.S. corporation)
PI US 2003020096 A1 20030130
US 6680260 B2 20040120
AI US 2002-244412 A1 20020917 (10)
RLI Division of Ser. No. US 2001-830389, filed on 26 Apr 2001, PENDING
PRAI JP 1999-240946 19990827
JP 2000-43764 20000222
DT Utility
FS APPLICATION
LREP OLIFF & BERRIDGE, PLC, P.O. BOX 19928, ALEXANDRIA, VA, 22320
CLMN Number of Claims: 28
ECL Exemplary Claim: 1
DRWN 8 Drawing Page(s)
LN.CNT 1187
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 21 OF 38 USPATFULL on STN
AB There is provided a method of producing a bonded SOI wafer wherein a silicon single crystal ingot is grown according to Czochralski method, the single crystal ingot is then sliced to produce a silicon single crystal wafer, the silicon single crystal wafer is subjected to heat treatment in a non-oxidizing atmosphere at a temperature of 1100° C. to 1300° C. for one minute or more and continuously to a heat treatment in an oxidizing atmosphere at a temperature of 700° C. to 1300° C. for one minute or more without cooling the wafer to a temperature less than 700° C. to provide a silicon single crystal wafer wherein a silicon oxide film

is formed on the surface, and the resultant wafer is used as the bond wafer, and a bonded SOI wafer produced by the method. There can be provided a SOI wafer that has a SOI layer having few crystal defects, good surface roughness and high quality in high productivity, in high yield and with low cost.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:326207 USPATFULL
TI Method of producing a bonded wafer and the bonded wafer
IN Akiyama, Shoji, Gunma, JAPAN
Tamatsuka, Masaro, Gunma, JAPAN
PA Shin-Etsu Handotal Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6492682 B1 20021210
WO 2001001427 20010104
AI US 2001-830389 20010426 (9)
WO 2000-JP5594 20000821
PRAI JP 1999-240946 19990827
JP 2000-43764 20000222
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nelms, David; Assistant Examiner: Vu, David
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 1
ECL Exemplary Claim: 1
DRWN 11 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 1045
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 22 OF 38 USPATFULL on STN
AB The present invention provides a silicon wafer sliced from a silicon single crystal ingot grown by the Czochralski method under such conditions that V-rich region should become dominant, wherein count number of particles having a size of 0.1 μm or more is 1 count/cm.sup.2 or less when particles are counted by using a particle counter and a method for producing a silicon single crystal. Thus, there is provided a production technique that can improve productivity and reduce cost for high quality silicon wafers of excellent device characteristics by further reducing density and size of defects such as COP.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:284777 USPATFULL
TI Silicon wafer and method for producing silicon single crystal
IN Hoshi, Ryoji, Fukushima, JAPAN
Fusegawa, Izumi, Fukushima, JAPAN
Ohta, Tomohiko, Fukushima, JAPAN
Maeda, Shigemaru, Fukushima, JAPAN
PI US 2002157598 A1 20021031
US 6632411 B2 20031014
AI US 2001-979519 A1 20011123 (9)
WO 2001-JP2451 20010327
PRAI JP 2000-92337 20000329
DT Utility
FS APPLICATION
LREP Oliff & Berridge, PO Box 19928, Alexandria, VA, 22320
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 705
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 23 OF 38 USPATFULL on STN
AB A single crystal silicon wafer comprising a front surface, a back surface, a lateral surface joining the front and back surfaces, a central axis perpendicular to the front and back surfaces, and a segment which is axially symmetric about the central axis extending substantially from the front surface to the back surface in which crystal lattice vacancies are the predominant intrinsic point defect, the segment having a radial width of at least about 25% of the radius and containing agglomerated vacancy defects and a residual concentration of crystal lattice vacancies wherein (i) the agglomerated vacancy defects have a radius of less than about 70 nm and (ii) the residual concentration of crystal lattice vacancy intrinsic point defects is less than the threshold concentration at which uncontrolled oxygen precipitation occurs upon subjecting the wafer to an oxygen precipitation heat treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:226110 USPATFULL
TI Process for preparing single crystal silicon having improved gate oxide integrity
IN Falster, Robert J., London, UNITED KINGDOM
Voronkov, Vladimir V., Merano, ITALY
Mutti, Paolo, Milan, ITALY
Bonoli, Fancesco, Novara, ITALY
PA MEMC Electronic Materials, Inc. (non-U.S. corporation)
PI US 2002121238 A1 20020905
US 6986925 B2 20060117
AI US 2002-39196 A1 20020102 (10)
PRAI US 2001-259362P 20010102 (60)
DT Utility
FS APPLICATION
LREP SENNIGER POWERS LEAVITT AND ROEDEL, ONE METROPOLITAN SQUARE, 16TH FLOOR, ST LOUIS, MO, 63102
CLMN Number of Claims: 59
ECL Exemplary Claim: 1
DRWN 17 Drawing Page(s)
LN.CNT 1985
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 24 OF 38 USPATFULL on STN
AB Epitaxial wafers showing marked IG effects can be manufactured from silicon single crystals doped or not doped with nitrogen without requiring any additional heat treatment process step while reducing the density of epitaxial layer defects. According to the first manufacturing method, an epitaxial layer is allowed to grow on the surface of a wafer sliced from a single crystal produced by employing a cooling rate of not less than 7.3° C./min in the temperature range of 1200-1050° C. in the step of pulling up thereof. According to the second manufacturing method, an epitaxial layer is allowed to grow on the surface of a silicon wafer sliced from a silicon single crystal doped with 1+10.sup.12 atoms/cm.sup.3 to 1+10.sup.14 atoms/cm.sup.3 as produced by employing a cooling rate of not less than 2.7° C./min in the temperature range of 1150-1020° C. and then a cooling rate of not more than 1.2° C./min in the temperature range of 1000-850° C. in the step of pulling up thereof.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:30419 USPATFULL
TI Method of manufacturing epitaxial wafer and method of producing single crystal as material therefor
IN Ono, Toshiaki, Saga, JAPAN
Tanaka, Tadami, Saga, JAPAN

Asayama, Eiichi, Saga, JAPAN
Nishikawa, Hideshi, Saga, JAPAN
Horai, Masataka, Saga, JAPAN
PA Sumitomo Metal Industries, Ltd., Osaka-shi, Japan (non-U.S. corporation)
PI US 2002017234 A1 20020214
US 6835245 B2 20041228
AI US 2001-883922 A1 20010620 (9)
PRAI JP 2000-188176 20000622
JP 2000-190631 20000626
DT Utility
FS APPLICATION
LREP ARMSTRONG,WESTERMAN, HATTORI,, MCLELAND & NAUGHTON, LLP, 1725 K STREET, NW, SUITE 1000, WASHINGTON, DC, 20006
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 1121
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 25 OF 38 USPATFULL on STN
AB A method of manufacturing a silicon wafer with robust gettering sites and a low concentration of surface defects is provided. The method comprises adding polycrystalline silicon to a crucible; adding a nitrogen-containing dopant to the crucible; heating the crucible to form a nitrogen-doped silicon melt; pulling a silicon crystal from the melt according to the Czochralski technique; forming a silicon wafer from the silicon crystal, wherein the silicon wafer includes a front surface and a back surface; placing the silicon wafer into a deposition chamber; heating the wafer; and simultaneously depositing an epitaxial first film of a desired compound onto the front surface of the wafer and a second film of the desired compound onto the back surface of the wafer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:138132 USPATFULL
TI Optimized silicon wafer gettering for advanced semiconductor devices
IN Dietze, Gerald R., Portland, OR, United States
Hanna, Sean G., Portland, OR, United States
Radzimski, Zbigniew J., Brush Prairie, WA, United States
PI US 2001015168 A1 20010823
US 6632277 B2 20031014
AI US 2001-759028 A1 20010111 (9)
RLI Continuation-in-part of Ser. No. US 2000-567659, filed on 9 May 2000, PENDING Continuation-in-part of Ser. No. US 1999-353196, filed on 14 Jul 1999, PENDING Continuation-in-part of Ser. No. US 1999-353197, filed on 14 Jul 1999, PENDING
DT Utility
FS APPLICATION
LREP KOLISCH HARTWELL DICKINSON MCCORMACK & H, EUSER, 520 S.W. YAMHILL STREET, SUITE 200, PORTLAND, OR, 97204
CLMN Number of Claims: 23
ECL Exemplary Claim: 1
DRWN 3 Drawing Page(s)
LN.CNT 729
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 26 OF 38 USPATFULL on STN
AB A low-cost method of manufacturing a silicon wafer is provided. The method comprises providing a crucible for melting silicon; adding silicon to the crucible; melting the silicon to form a melt; applying an electrical potential across the crucible; pulling a silicon crystal from the melt according to the Czochralski technique

at a pulling rate of greater than 1.1 mm/min; and forming a silicon wafer from the silicon crystal. The method may also include adding a nitrogen-containing dopant to the crucible. Furthermore, the method may include etching the wafer first in an alkaline etching solution, and then in an acidic etching solution. The method may also include simultaneously depositing an epitaxial first film on the frontside of the wafer and a second film on the backside of the wafer, wherein the second film traps impurities on the backside of the wafer so the impurities do not contaminate the frontside of the wafer while the epitaxial first film is being grown.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:109358 USPATFULL
TI High efficiency silicon wafer optimized for advanced semiconductor devices
IN Dietze, Gerald R., Portland, OR, United States
Hanna, Sean G., Portland, OR, United States
Radzimski, Zbigniew J., Brush Prairie, WA, United States
PA SEH America, Inc. (U.S. corporation)
PI US 2001007240 A1 20010712
US 6454852 B2 20020924
AI US 2001-759030 A1 20010111 (9)
RLI Continuation-in-part of Ser. No. US 2000-567659, filed on 9 May 2000, PENDING Continuation-in-part of Ser. No. US 1999-353196, filed on 14 Jul 1999, PENDING Continuation-in-part of Ser. No. US 1999-353197, filed on 14 Jul 1999, PENDING
DT Utility
FS APPLICATION
LREP Kolisch, Hartwell, Dickinson, McCormack & Heuser, 200 Pacific Building, 520 S.W. Yamhill Street, Portland, OR, 97204
CLMN Number of Claims: 31
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 917
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 27 OF 38 USPATFULL on STN
AB There are disclosed a method for producing an SOI substrate comprising forming an oxide layer on a surface of at least one silicon wafer among two silicon wafers, closely contacting one wafer with the other wafer so that the oxide layer should be interposed between them, subjecting the wafers to a heat treatment to firmly bond the wafers, and making a device processing side wafer thinner to a desired thickness, wherein a silicon single crystal wafer obtained by growing a silicon single crystal ingot doped with nitrogen by the Czochralski method, and slicing the single crystal ingot into a silicon single crystal wafer is used as the device processing side wafer, and an SOI substrate produced by the method. The present invention provides a method for producing SOI substrates, in particular thin film SOI substrates having an SOI layer thickness of 1 μm or less, exhibiting a small crystal defect size in the SOI layer, and SOI substrates with low cost and high productivity.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:63046 USPATFULL
TI Method for producing SOI substrate and SOI substrate
IN Tamatsuka, Masaro, Gunma-ken, Japan
PA Shin-Etsu Handotai Co., Ltd., Tokyo, Japan (non-U.S. corporation)
PI US 6224668 B1 20010501
AI US 1999-313858 19990518 (9)

PRAI JP 1998-169309 19980602
DT Utility
FS Granted
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Hogan & Hartson, LLP
CLMN Number of Claims: 14
ECL Exemplary Claim: 1
DRWN 2 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 718
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 28 OF 38 USPAT2 on STN
AB There is provided a method for manufacturing a silicon wafer or a silicon epitaxial wafer capable of imparting an excellent IG capability thereto in a stable manner by simultaneously realizing higher density of oxide precipitates and larger sizes thereof at a stage prior to a device fabrication process. The present invention is a method for manufacturing a silicon wafer wherein the silicon wafer is subjected to heat treatment to impart a gettering capability thereto comprising at least the following three steps of: a temperature raising step A for generating oxygen precipitation nuclei; a temperature raising step B for growing the oxygen precipitation nuclei; and a constant temperature keeping step C for growing the oxygen precipitation nuclei into oxide precipitates of larger sizes.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:221464 USPAT2
TI Methods for manufacturing silicon wafer and silicone epitaxial wafer, and silicon epitaxial wafer
IN Takeno, Hiroshi, Annaka, JAPAN
PA Shin-Etsu Handotai Co., Ltd., JAPAN (non-U.S. corporation)
PI US 7033962 B2 20060425
WO 2003009365 20030130
AI US 2002-482843 20020530 (10)
WO 2002-JP5000 20020530
20040106 PCT 371 date
PRAI JP 2001-209160 20010710
JP 2001-296743 20010927
JP 2001-296744 20010927
JP 2001-296745 20010927
DT Utility
FS GRANTED
EXNAM Primary Examiner: Geyer, Scott
LREP Rader, Fishman & Grauer PLLC
CLMN Number of Claims: 9
ECL Exemplary Claim: 1
DRWN 37 Drawing Figure(s); 14 Drawing Page(s)
LN.CNT 2414
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 29 OF 38 USPAT2 on STN
AB The present invention provides a silicon single crystal wafer having a diameter of 300 mm or more and having a defect-free layer containing no COP for a depth of 3 μm or more from a surface and a method for producing a silicon single crystal, wherein, when a silicon single crystal having a diameter of 300 mm or more is pulled with nitrogen doping by the CZ method, the crystal is grown with a value of V/G [mm.sup.2/K.multidot.min] of 0.17 or less, where V [mm/min] is a pulling rate, and G [K/mm] is an average of temperature gradient in the crystal along a pulling axis from the melting point of silicon to 1400° C. Thus, there are established conditions for pulling a silicon single crystal and conditions for heat treatment of

wafer for obtaining a silicon single crystal wafer having a defect-free layer free from COP for a sufficient depth of the surface layer by pulling a silicon single crystal having a diameter of 300 mm or more, processing the crystal into wafers and subjecting the wafers to the heat treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:248088 USPAT2

TI Silicon single crystal wafer having void denuded zone on the surface and diameter of above 300 mm and its production method

IN Iida, Makoto, Gunma, JAPAN

PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)

PI US 6902618 B2 20050607
WO 2002010390 20021227

AI US 2003-344423 20020607 (10)
WO 2002-JP5692 20020607
20030212 PCT 371 date

PRAI JP 2001-181587 20010615

DT Utility

FS GRANTED

EXNAM Primary Examiner: Hiteshew, Felisa

LREP Hogan & Hartson, LLP

CLMN Number of Claims: 6

ECL Exemplary Claim: 1

DRWN 0 Drawing Figure(s); 0 Drawing Page(s)

LN.CNT 446

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 30 OF 38 USPAT2 on STN

AB According to the present invention, there are provided a method for producing a silicon single crystal wafer which contains oxygen induced defects by subjecting a silicon single crystal wafer containing interstitial oxygen to a heat treatment wherein the heat treatment includes at least a step of performing a heat treatment using a resistance-heating type heat treatment furnace and a step of performing a heat treatment using a rapid heating and rapid cooling apparatus, and a silicon single crystal wafer produced by the method. There can be provided a method for producing a silicon single crystal wafer which has a DZ layer of higher quality compared with a conventional wafer in a wafer surface layer part and has oxygen induced defects at a sufficient density in a bulk part and the silicon single crystal wafer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AN 2003:235983 USPAT2

TI Method for manufacturing single-crystal-silicon wafers

IN Kobayashi, Norihiro, Gunma, JAPAN
Tamatsuka, Masaro, Gunma, JAPAN
Nagoya, Takatoshi, Gunma, JAPAN

PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)

PI US 6805743 B2 20041019
WO 2002011196 20020207

AI US 2003-333970 20030124 (10)
WO 2001-JP6274 20010719

PRAI JP 2000-229522 20000728

DT Utility

FS GRANTED

EXNAM Primary Examiner: Hiteshew, Felisa

LREP Hogan & Hartson LLP
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 2 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 580
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 31 OF 38 USPAT2 on STN
AB A silicon semiconductor substrate which realizes a defect-free region of void type crystals to a greater depth and allows the duration of production to be decreased and a method for the production thereof are provided. A silicon semiconductor substrate derived from a silicon single crystal grown by the Czochralski method or the magnetic field-applied Czochralski method, which is obtainable by using a silicon semiconductor substrate satisfying the relational expression, 0.2≥V/S/R, providing V denotes the volume of void type defects, S denotes the surface area thereof, and R denotes the radius of spherical defects presumed to have the same volume as the void defects having the volume of V, and heat treating this substrate at a temperature exceeding 1150° C.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:194709 USPAT2
TI Silicon semiconductor substrate and method for production thereof
IN Tachikawa, Akiyoshi, Yamaguchi, JAPAN
Ishisaka, Kazunori, Yamaguchi, JAPAN
PA Wacker Siltronic Gesellschaft Fur Halbleiter Materialien AG, Burghausen, GERMANY, FEDERAL REPUBLIC OF (non-U.S. corporation)
PI US 6767848 B2 20040727
AI US 2002-241180 20020911 (10)
PRAI JP 2001-280460 20010914
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nhu, David
LREP Collard & Roe, P.C.
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 0 Drawing Figure(s); 0 Drawing Page(s)
LN.CNT 1012
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 32 OF 38 USPAT2 on STN
AB According to the present invention, there is disclosed a silicon single crystal wafer grown according to the CZ method which is a wafer having a diameter of 200 mm or more produced from a single crystal grown at a growth rate of 0.5 mm/min or more without doping except for a dopant for controlling resistance, wherein neither an octahedral void defect due to vacancies nor a dislocation cluster due to interstitial silicons exists as a grown-in defect, and a method for producing it. There can be provided a high quality silicon single crystal wafer having a large diameter wherein a silicon single crystal in which both of octahedral void defects and dislocation clusters which are growth defects are substantially eliminated is grown at higher rate compared with the conventional method by the usual CZ method, and furthermore by controlling a concentrations of interstitial oxygen in the crystal to be low, a precipitation amount is lowered and ununiformity of BMD in a plane of the wafer is improved, and provided a method for producing it.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:156882 USPAT2

TI Silicon single crystal wafer and
method for manufacturing the same
IN Fusegawa, Izumi, Fukushima, JAPAN
Kitagawa, Koji, Fukushima, JAPAN
Hoshi, Ryoji, Fukushima, JAPAN
Sakurada, Masahiro, Fukushima, JAPAN
Ohta, Tomohiko, Fukushima, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6893499 B2 20050517
WO 2002002852 20020110
AI US 2002-312921 20010628 (10)
WO 2001-JP5565 20010628
20021226 PCT 371 date
PRAI JP 2000-199226 20000630
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Hogan & Hartson, LLP
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 6 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 983
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 33 OF 38 USPAT2 on STN
AB An improved method of obtaining a wafer exhibiting high resistivity and high gettering effect while preventing the reduction of resistivity due to the generation of oxygen donors provided by: a) using the CZ method to grow a silicon single crystal ingot having a resistivity of 100 Ω.multidot.cm or more, preferably 1000 Ω.multidot.cm, and an initial interstitial oxygen concentration of 10 to 40 ppma while doping the crystal with an electrically inactive material such as nitrogen, carbon, or tin, b) processing the ingot into a wafer, and c) subjecting the wafer to an oxygen precipitation heat treatment whereby the residual interstitial oxygen content in the wafer is reduced to about 8 ppma or less.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:156880 USPAT2
TI High resistivity silicon wafer having electrically inactive dopant and method of producing same
IN Kononchuk, Oleg V., Brush Prairie, WA, United States
Koveshnikov, Sergei V., Vancouver, WA, United States
Radzimski, Zbigniew J., Brush Prairie, WA, United States
Weaver, Neil A., Battle Ground, WA, United States
PA SEH America, Inc., Vancouver, WA, United States (U.S. corporation)
PI US 6673147 B2 20040106
AI US 2001-8404 20011206 (10)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
LREP Alston & Bird LLP
CLMN Number of Claims: 33
ECL Exemplary Claim: 1
DRWN 1 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 693
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 34 OF 38 USPAT2 on STN
AB There is provided a method of producing a bonded SOI wafer wherein a silicon single crystal ingot is grown according to Czochralski method, the single crystal ingot is then sliced to produce a

silicon single crystal wafer, the silicon single crystal wafer is subjected to heat treatment in a non-oxidizing atmosphere at a temperature of 1100° C. to 1300° C. for one minute or more and continuously to a heat treatment in an oxidizing atmosphere at a temperature of 700° C. to 1300° C. for one minute or more without cooling the wafer to a temperature less than 700° C. to provide a silicon single crystal wafer wherein a silicon oxide film is formed on the surface, and the resultant wafer is used as the bond wafer, and a bonded SOI wafer produced by the method. There can be provided a SOI wafer that has a SOI layer having few crystal defects, good surface roughness and high quality in high productivity, in high yield and with low cost.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:28176 USPAT2
TI Method of producing a bonded wafer and the bonded wafer
IN Akiyama, Shoji, Gunma, JAPAN
Tamatsuka, Masaro, Gunma, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6680260 B2 20040120
AI US 2002-244412 20020917 (10)
RLI Division of Ser. No. US 2001-830389, filed on 26 Apr 2001, now patented, Pat. No. US 6492682
PRAI JP 1999-240946 19990827
JP 2000-43764 20000222
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nelms, David; Assistant Examiner: Vu, David
LREP Oliff & Berridge, PLC
CLMN Number of Claims: 28
ECL Exemplary Claim: 1
DRWN 11 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 1169
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 35 OF 38 USPAT2 on STN
AB The present invention provides a silicon wafer sliced from a silicon single crystal ingot grown by the Czochralski method under such conditions that V-rich region should become dominant, wherein count number of particles having a size of 0.1 μm or more is 1 count/cm.sup.2 or less when particles are counted by using a particle counter and a method for producing a silicon single crystal. Thus, there is provided a production technique that can improve productivity and reduce cost for high quality silicon wafers of excellent device characteristics by further reducing density and size of defects such as COP.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:284777 USPAT2
TI Silicon wafer and method for producing silicon single crystal
IN Hoshi, Ryoji, Fukushima, JAPAN
Fusegawa, Izumi, Fukushima, JAPAN
Ohta, Tomohiko, Fukushima, JAPAN
Maeda, Shigemaru, Fukushima, JAPAN
PA Shin-Etsu Handotai Co., Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6632411 B2 20031014
WO 2001073169 20011004
AI US 2001-979519 20011123 (9)
WO 2001-JP2451 20010327

PRAI JP 2000-92337 20000329
DT Utility
FS GRANTED
EXNAM Primary Examiner: Hiteshew, Felisa
CLMN Number of Claims: 20
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 723
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 36 OF 38 USPAT2 on STN
AB A single crystal silicon wafer comprising a front surface, a back surface, a lateral surface joining the front and back surfaces, a central axis perpendicular to the front and back surfaces, and a segment which is axially symmetric about the central axis extending substantially from the front surface to the back surface in which crystal lattice vacancies are the predominant intrinsic point defect, the segment having a radial width of at least about 25% of the radius and containing agglomerated vacancy defects and a residual concentration of crystal lattice vacancies wherein (i) the agglomerated vacancy defects have a radius of less than about 70 nm and (ii) the residual concentration of crystal lattice vacancy intrinsic point defects is less than the threshold concentration at which uncontrolled oxygen precipitation occurs upon subjecting the wafer to an oxygen precipitation heat treatment.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:226110 USPAT2
TI Single crystal silicon having improved gate oxide integrity
IN Falster, Robert J., London, UNITED KINGDOM
Voronkov, Vladimir V., Merano, ITALY
Mutti, Paolo, Milan, ITALY
Bonoli, Francesco, Novara, ITALY
PA MEMC Electronic Materials, Inc., St. Peters, MO, UNITED STATES (U.S. corporation)
PI US 6986925 B2 20060117
AI US 2002-39196 20020102 (10)
PRAI US 2002-259362P 20020102 (60)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Pyon, Harold; Assistant Examiner: Rhee, Jane
LREP Senniger Powers
CLMN Number of Claims: 27
ECL Exemplary Claim: 1
DRWN 20 Drawing Figure(s); 17 Drawing Page(s)
LN.CNT 1866
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 37 OF 38 USPAT2 on STN
AB Epitaxial wafers showing marked IG effects can be manufactured from silicon single crystals doped or not doped with nitrogen without requiring any additional heat treatment process step while reducing the density of epitaxial layer defects. According to the first manufacturing method, an epitaxial layer is allowed to grow on the surface of a wafer sliced from a single crystal produced by employing a cooling rate of not less than 7.3° C./min in the temperature range of 1200-1050° C. in the step of pulling up thereof. According to the second manufacturing method, an epitaxial layer is allowed to grow on the surface of a silicon wafer sliced from a silicon single crystal doped with 1+10.sup.12 atoms/cm.sup.3 to 1+10.sup.14 atoms/cm.sup.3 as produced by employing a cooling rate of not less than 2.7° C./min

in the temperature range of 1150-1020° C. and then a cooling rate of not more than 1.2° C./min in the temperature range of 1000-850° C. in the step of pulling up thereof.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:30419 USPAT2
TI Method of manufacturing epitaxial wafer and method of producing single crystal as material therefor
IN Ono, Toshiaki, Saga, JAPAN
Tanaka, Tadami, Saga, JAPAN
Asayama, Eiichi, Saga, JAPAN
Nishikawa, Hideshi, Saga, JAPAN
Horai, Masataka, Saga, JAPAN
PA Sumitomo Mitsubishi Silicon Corporation, Tokyo, JAPAN (non-U.S. corporation)
PI US 6835245 B2 20041228
AI US 2001-883922 20010620 (9)
PRAI JP 2000-188176 20000622
JP 2000-190631 20000626
DT Utility
FS GRANTED
EXNAM Primary Examiner: Norton, Nadine G.; Assistant Examiner: Anderson, Matthew A.
LREP Westerman, Hattori, Daniels & Adrian, LLP
CLMN Number of Claims: 5
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 1049
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 38 OF 38 USPAT2 on STN
AB A low-cost method of manufacturing a silicon wafer is provided. The method comprises providing a crucible for melting silicon; adding silicon to the crucible; melting the silicon to form a melt; applying an electrical potential across the crucible; pulling a silicon crystal from the melt according to the Czochralski technique at a pulling rate of greater than 1.1 mm/min; and forming a silicon wafer from the silicon crystal. The method may also include adding a nitrogen-containing dopant to the crucible. Furthermore, the method may include etching the wafer first in an alkaline etching solution, and then in an acidic etching solution. The method may also include simultaneously depositing an epitaxial first film on the frontside of the wafer and a second film on the backside of the wafer, wherein the second film traps impurities on the backside of the wafer so the impurities do not contaminate the frontside of the wafer while the epitaxial first film is being grown.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2001:109358 USPAT2
TI High efficiency silicon wafer optimized for advanced semiconductor devices
IN Dietze, Gerald R., Portland, OR, United States
Hanna, Sean G., Portland, OR, United States
Radzimski, Zbigniew J., Brush Prairie, WA, United States
PA SEH America, Inc., Vancouver, WA, United States (U.S. corporation)
PI US 6454852 B2 20020924
AI US 2001-759030 20010111 (9)
RLI Continuation-in-part of Ser. No. US 2000-567659, filed on 9 May 2000
Continuation-in-part of Ser. No. US 1999-353196, filed on 14 Jul 1999, now abandoned Continuation-in-part of Ser. No. US 1999-353197, filed on 14 Jul 1999
DT Utility
FS GRANTED

EXNAM Primary Examiner: Hiteshew, Felisa
LREP   Alston & Bird LLP
CLMN   Number of Claims: 33
ECL   Exemplary Claim: 1
DRWN   10 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 939
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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Day : Friday
Date: 7/21/2006

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Time: 10:45:52

Inventor Name Search Result

Your Search was:

Last Name = HOSHI
First Name = RYOJI

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07950677	5302832	250	09/25/1992	METHOD FOR EVALUATION OF SPATIAL DISTRIBUTION OF DEEP LEVEL CONCENTRATION IN SEMICONDUCTOR CRYSTAL	HOSHI, RYOJI
08524453	5598452	250	09/06/1995	METHOD OF EVALUATING A SILICON SINGLE CRYSTAL	HOSHI, RYOJI
08557563	5612539	250	11/14/1995	METHOD OF EVALUATING LIFETIME RELATED QUALITY OF SEMICONDUCTOR SURFACE	HOSHI, RYOJI
09270453	6156119	150	03/17/1999	SILICON SINGLE CRYSTAL AND METHOD FOR PRODUCING THE SAME	HOSHI, RYOJI
09290261	6117231	150	04/13/1999	METHOD OF MANUFACTURING SEMICONDUCTOR SILICON SINGLE CRYSTAL WAFER	HOSHI, RYOJI
09646713	6565822	150	09/21/2000	EPITAXIAL SILICON WAFER, METHOD FOR PRODUCING THE SAME AND SUBTRATE FOR EPITAXIAL SILICON WAFER	HOSHI, RYOJI
09937132	6632280	150	09/21/2001	SINGLE CRYSTAL GROWING DEVICE	HOSHI, RYOJI
09959381	6592662	150	10/24/2001	METHOD FOR PREPARING SILICON SINGLE CRYSTAL AND SILICON SINGLE CRYSTAL	HOSHI, RYOJI
09979519	6632411	150	11/23/2001	SILICON WAFER AND METHOD FOR PRODUCING SILICON SINGLE CRYSTAL	HOSHI, RYOJI
10204278	6764548	150	08/20/2002	APPARATUS AND METHOD	HOSHI, RYOJI

				FOR PRODUCING SILICON SEMICONDUCTOR SINGLE CRYSTAL	
10312921	6893499	150	12/26/2002	SILICON SINGLE CRYSTAL WAFER AND METHOD FOR MANUFACTURING THE SAME	HOSHI, RYOJI
10503721	Not Issued	41	08/06/2004	HEATER FOR MANUFACTURING A CRYSTAL	HOSHI, RYOJI
10520099	Not Issued	30	01/04/2005	A Silicon Wafer For Epitaxial Growth, An Epitaxial Wafer, And A Method For Producing It	HOSHI, RYOJI
10525244	Not Issued	20	02/22/2005	Single crystal, single crystal wafer, epitaxial wafer, and method of growing single crystal	HOSHI, RYOJI
10550088	Not Issued	20	09/20/2005	Process for producing single crystal	HOSHI, RYOJI
10573822	Not Issued	19	01/01/0001	A method for producing a single crystal	HOSHI, RYOJI

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = SONOKAWA
First Name = SUSUMU

Application#	Patent#	Status	Date Filed	Title	Inventor Name
07593920	Not Issued	166	10/05/1990	METHOD OF ADJUSTING CONCENTRATION OF OXYGEN IN SILICON SINGLE CRYSTAL AND APPARATUS FOR USE IN THE METHOD	SONOKAWA, SUSUMU
07614760	5131974	150	11/16/1990	METHOD OF CONTROLLING OXYGEN CONCENTRATION IN SINGLE CRYSTAL AND AN APPARATUS THEREFOR	SONOKAWA, SUSUMU
07825443	5269875	150	01/24/1992	METHOD OF ADJUSTING CONCENTRATION OF OXYGEN IN SILICON SINGLE CRYSTAL AND APPARATUS FOR USE IN THE METHOD	SONOKAWA, SUSUMU
08776776	5972106	150	02/10/1997	DEVICE AND METHOD FOR PRODUCING SINGLE CRYSTAL	SONOKAWA, SUSUMU
08786340	5882398	250	01/23/1997	METHOD OF MANUFACTURING SINGLE CRYSTAL OF SILICON	SONOKAWA, SUSUMU
09362103	6228165	150	07/28/1999	METHOD OF MANUFACTURING CRYSTAL OF SILICON USING AN ELECTRIC POTENTIAL	SONOKAWA, SUSUMU
09646713	6565822	150	09/21/2000	EPITAXIAL SILICON WAFER, METHOD FOR PRODUCING THE SAME AND SUBTRATE FOR EPITAXIAL SILICON WAFER	SONOKAWA, SUSUMU
09959302	6506251	150	10/23/2001	METHOD FOR PRODUCING SILICON SINGLE CRYSTAL	SONOKAWA, SUSUMU
10503721	Not Issued	41	08/06/2004	HEATER FOR MANUFACTURING A CRYSTAL	SONOKAWA, SUSUMU

10520099	Not Issued	30	01/04/2005	A Silicon Wafer For Epitaxial Growth, An Epitaxial Wafer, And A Method For Producing It	SONOKAWA, SUSUMU
10525244	Not Issued	20	02/22/2005	Single crystal, single crystal wafer, epitaxial wafer, and method of growing single crystal	SONOKAWA, SUSUMU
10550088	Not Issued	20	09/20/2005	Process for producing single crystal	SONOKAWA, SUSUMU

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** Sonokawa **First Name** Susumu Search

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